

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

ULRICH BORTFELD

Application No.: 10/816,144

Filed: March 31, 2004

For: **INSTRUCTION-WORD ADDRESSABLE  
L0 INSTRUCTION CACHE**



Art Group: 2186

Examiner: Lev Iwashko

**INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a final Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

06/19/2006 CNGUYEN2 00000056 10816144

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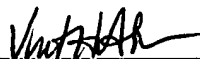
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The fee set in the amount of \$180.00 for submission of the Information Disclosure Statement is enclosed herewith. Please charge any additional fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: June 15, 2006



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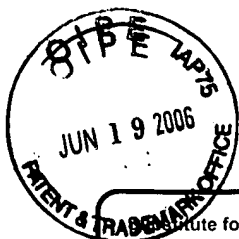
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06-15-06

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Substitute for form 1449A/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				Application Number	10/816,144
				Filing Date	March 31, 2004
				First Named Inventor	Ulrich Bortfeld
				Art Unit	2186
				Examiner Name	Lev Iwashko
				Attorney Docket Number	42P19079
Sheet	1	of	1		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		RAMINDER S. BAJWA ET AL., "Instruction Buffering to Reduce Power in Processors for Signal Processing", <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , Vol. 5, No. 4, December 1997, pg. 417-424.	
		PAUL WANG LEE, "Trace Cache", EE482: Advanced Computer Organization, Lecture #5, Processor Architecture, <i>Stanford University</i> , May 10, 2000, pg. 1-4.	
		PAUL W. LEE, "Exploring the Trace Cache Design Space", EE482a - Prof. William Dally, <i>Stanford University</i> , May 30, 2000, pg. 1-14.	
		CHANGWOO JUNG ET AL., "Instruction Cache Organisation for Embedded Low-Power Processors", <i>Electronics Letters</i> , Vol. 37, No. 9, April 26, 2001, pg. 554-555.	

Examiner Signature	Date Considered
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\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

†Applicant's unique citation designation number:²Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08B (08-03) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 08/11/2003.  
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